Mark schemes

Q1.

(a) When B = logic 0, (point D is logic 1.) (Result: closes the lower AND gate and opens the upper AND gate.) Only the 1024 Hz signal is allowed to (pass through to the OR gate) output Q. ✓

1st mark:
- *explanation for either logic 1 or logic 0 input*
- *reference as to which frequency passes through OR gate.*

When B = logic 1,(point D is logic 0). (Result: closes the upper AND gate and opens the lower AND gate.) Only the 512 Hz signal is allowed to (pass through to the OR gate) output Q. ✓

2nd mark:
reference to other half of the cycle and output frequency.

1 Max if there is no reference to the action of at least 1 gate.

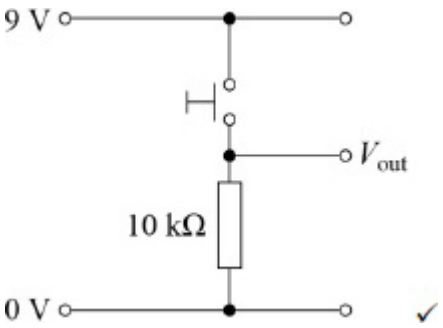
2

(b) **Q** = (A . $\overline{B}$) + (B . C) ✓ ✓

1st mark for: contents of either bracket
2nd mark for: contents of other bracket and the '+'

2

(c)



Mark awarded if all the following are present:
- *resistor and push-to-make switch are in correct position*
- *output point in correct position and labelled.*

1

(d) Q_9 ✓

$2^{(n+1)} = 1024$

Condone n = 9

1

(e) Option 1 requires a total of 6 ICs whereas Option 2 requires a total of 3 ICs ✓

Advantage: One from: ✓

- smaller circuit to fit toys
- less power consumed / extended battery life
- less complex circuits / lower production costs

1st mark: identifies the main advantage (must be numerical)

2nd mark: gives one advantage from the list /or other valid explanation

*Allow one mark for answers that only consider number of **logic gates** in the two systems leading to the correct conclusion.*

2

[8]

Q2.

(a) 1 from ✓

- 160 × 7 = 1120 bits
- 140 bytes seen
- their number of bits ÷ (64×10^3)
- their number of bytes ÷ (8×10^3)

1st mark for correct bits or bytes conversion in message or time calculation

= 17.5×10^{-3} s ✓

2nd mark for answer

Allow 2 sf answer.

2

(b) Internal noise:
thermal agitation of electrons / charge carriers in a conductor

Accept one example for the mark

OR

External noise:
idea of electromagnetic interference (EMI) eg cross-talk / power switching etc. ✓

1

(c) Effect of electrical noise on the signal:

- degrades the quality of the signal ✓

Effect of electrical noise on the communication system:

- reduces the efficiency of the transmission e.g. increased latency of the system ✓

2

(d)

Figure 6

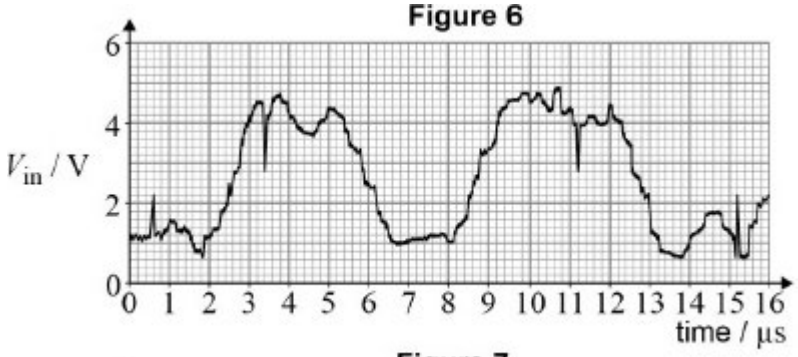
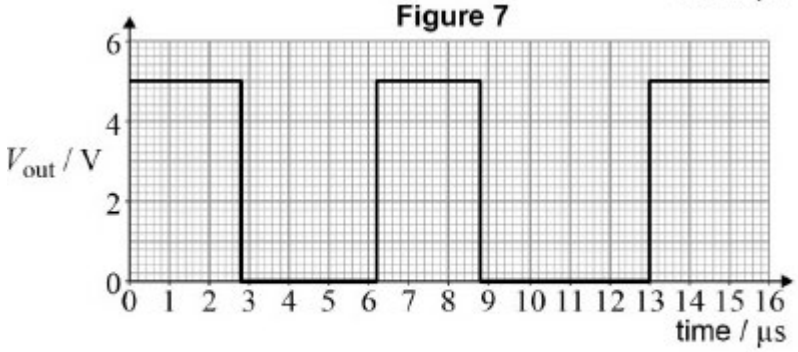


Figure 7



✓✓

1st mark - 0 to 5 V sq wave with 3 marks and two spaces

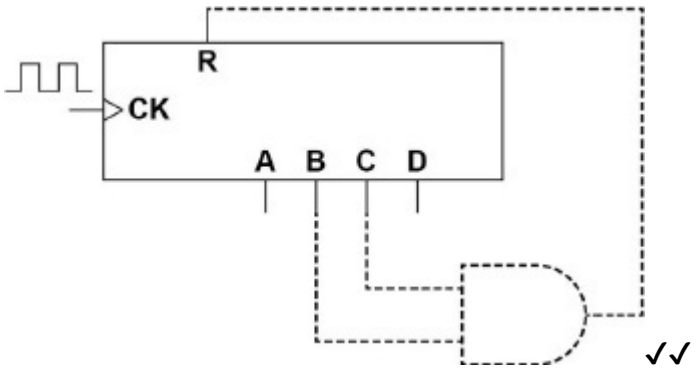
2nd mark - any three correct transitions.

2

[7]

Q3.

(a)



✓✓

1 mark for use of the correct counter outputs

1 mark for the correct logic gate connected to reset ***R***

2

(b) input **C**
segment **b** ✓

Both input and segment needed for the mark

Do not allow ***B*** *for* ***b***

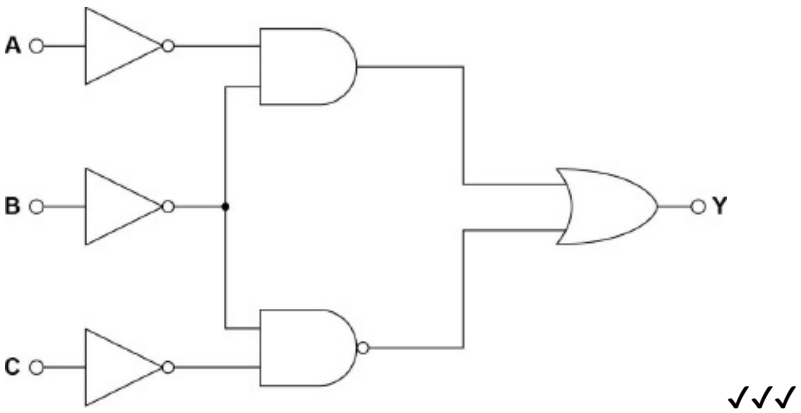
1

(c) **f** ✓

Allow ***F*** *for* ***f***

1

(d)



✓✓✓

MP1*: all inputs inverted (accept a shorted-out NAND or NOR gates for the inverters)*

MP2: *for correct use of AND and NAND*

Condone a NOT following an AND for the NAND gate.

MP3: *for final gate being OR*

3

[7]

Q4.

(a) $\bar{A}$ ✓

. B ✓

$\bar{A}$. **B** ✓

Do not allow $\overline{A + B}$

2

(b) EOR ✓

Accept: XOR ; EXOR; Exclusive OR gate

1

(c)

B	A	C	D	E	X	Y	Z
0	0	1	1	0	0	1	0
0	1	0	1	1	0	0	1
1	0	1	0	1	1	0	0
1	1	0	0	0	0	1	0

X and **Z** correct ✓

Y correct ✓

2

(d) NOR gate ✓

Also accept any of:
EXNOR; ENOR; XNOR; Exclusive NOR gate

1

(e)

X	Y	Z	
A = B	A < B	A > B	
A < B	A = B	A > B	✓
A < B	A > B	A = B	
A > B	A = B	A < B	

1

[7]

Q5.

(a)
- When V_c reaches a value of V_u, the output voltage V_{out} drops LOW. ✓
- The capacitor now discharges through the resistor causing the value of V_c to fall. ✓
- When V_c reaches a value of V_L, the output voltage V_{out} jumps HIGH. ✓

3

(b) **Mark-to-space ratio**

R_B gets smaller and hence (t_H) is reduced

OR

R_A gets bigger and hence (t_L) is increased ✓

First mark: Either statement or equivalent labelled diagram(s).

Hence mark:space ratio is reduced / smaller ✓

Second mark: Conclusion

PRF = $\frac{1}{T} = \frac{1}{(t_H + t_L)} = \frac{1}{0.7C\,(2R+R_A+R_B)}$

The total resistance ($2R + R_A + R_B$) is constant ✓

As a result of a constant resistance in the circuit, PRF does not change ✓

First mark: explanation of how total resistance in the circuit affects the periodic time

Second mark: Conclusion.

4

[7]